

Steffen Vogel

Curriculum Vitae

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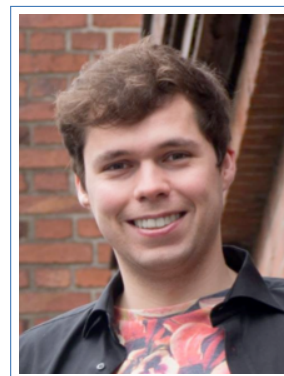
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Personal Data

Date of Birth March 20th, 1990, Baden, Switzerland

Nationality German

Family Status Single

Experiences

05.2017 – currently **Research Associate**, *Distributed real-time simulation*, Institute for Automation of Complex Power Systems, RWTH Aachen University
Pursuing PhD degree under the supervision of Prof. Antonello Monti.

Achievements:

- **Global-RT SuperLab Demo** an inter-continental GD-RTS experiment lead by RWTH & Idaho National Lab with 8 participating laboratories and a total of 10 distributed real-time simulators.
- Lead developer of **VILLASframework**, open-source framework for locally and geographically distributed real-time simulation (GD-RTS).
 - Management and coordination of development process
 - Support for over 30 institutional users, world-wide.
- Lead developer and project manager of **RWTHjupyter**, a scalable online platform for interactive computing in teaching at University-level.
- Internal project-lead of **Urban Energy Lab 2.0 - RTlab**
 - Extension of RWTH-ACS real-time laboratory with a high 6-digit budget
 - Equipment acquisition, installation & integration into existing real-time simulation infrastructure
 - Development of cross-vendor hard real-time interconnects for digital real-time simulators.
- Internal project-lead of the **Jupyter4Power** project
 - Integration of RWTHjupyter service into European and global authentication federations (DFN-AAI, eduGain).
- Internal project-lead of the **ERIGrid 2.0** project
 - Participant in two Transnational Access exchanges as part of former ERIGrid 1 project
 - Work-package leader of Virtual Access programme in ERIGrid 2.0

10.2019 – 11.2019 **Research Visit**, *Technical University of Denmark, Department of Electrical Engineering, PowerLabDK / SYSLAB*

Transnational Access Exchange "VILLAS4ERIGrid" as part of ERIGrid 1 H2020 project.

- 06.2019 – 07.2019 **Research Visit**, *SINTEF, Trondheim, Norway*, SINTEF Smart Grid Laboratory
Transnational Access Exchange as part of Marinet H2020 project.
- 04.2019 – 05.2019 **Research Visit**, *TU Delft, Intelligent Electrical Power Grids Group*, Real Time Digital Simulator (RTDS) Lab
Transnational Access Exchange "VILLAS4ERIGrid" as part of ERIGrid 1 H2020 project.
- 04.2014 – 07.2016, 02.2017 – 04.2017 **Student Assistant**, *Internet distributed power grid simulation*, Institute for Automation of Complex Power Systems, RWTH Aachen University
Implementing real-time communication tools based on RT-Linux, OPAL-RT and RTDS simulators. Supervisor: M.Sc. Marija Stevic
- 08.2016 – 01.2017 **Intern**, *FPGA modelling*, eFPGAsim team, OPAL-RT Technologies Inc.
Extending, testing and packaging the electric hardware solver (eHS), a FPGA-based EMTP solver.
- 04.2014 – 08.2014 **Exercise Instructor**, *Hands-on sessions computer science 4*, Chair for Operating Systems, RWTH Aachen University
Undertaking exercises on system / parallel programming, x86-Assembly and more.
- 10.2011 – 04.2012 **Student Tutor**, *C / C++ programming laboratory*, Institute for Man-Machine Interaction, RWTH Aachen University
Supervising a practical course on C / C++ programming.
- 09.2011 – 08.2013 **Student Lecturer**, *Micro controller study group*, Institute for Man-Machine Interaction, RWTH Aachen University
Giving introductory lectures on micro controller programming based on the Atmel ATmega family.

Voluntary commitment

- 05.2011 – 05.2012 **Presidency**, *ROCK YOUR LIFE! Aachen e.V.*, Aachen
Foundation and organization of a nonprofit association. RYL unites students and pupils in mentoring relations to support them in their succession planning, job-seeking and more.
- 08.2009 – 08.2010 **Voluntary year (FöJ)**, *KATALYSE Institut e.V.*, Cologne
FöJ in Germany: gap year taken to work as a volunteer in environmental projects.

Education

- 10.2014 – Present **M.Sc. Electrical Engineering, Information Technology and Computer Engineering**, *RWTH University, Aachen*
with major field of studies Computer Engineering
- 10.2010 – 10.2014 **B.Sc. Electrical Engineering, Information Technology and Computer Engineering**, *RWTH University, Aachen*, Final grade¹: 2.8
with major field of studies Computer Engineering
- 08.2001 – 06.2009 **Abitur**, *Justus-Liebig-Schule*, Darmstadt, Final grade: 2.2
Gymnasium²
- 1997 – 2001 **Elementary school**, *Schillerschule*, Griesheim

ICT Skills

Programming Languages C / C++, Go, Python, Matlab, VHDL, Javascript, TCL & Bash scripting

¹All grades are in the German grading system: 1.0 = 100 %, 5.0 < 50 %

²Diploma from German secondary school qualifying for university admission or matriculation.

Toolchains & Libraries	Xilinx System Generator, ISE & Vivado, Jupyter, GNU GCC & Core / Bin-utils, Yocto Linux / OpenEmbedded, Qt, OpenCV, OpenMP
Environments	Git, Make, CMake
Operating Systems	Linux, macOS, Windows
System Administration	Advanced Linux-system Administration, Ansible, Docker, Kubernetes, Helm, Bird routing daemon, iproute2, netfilter
Web	HTML, CSS, Javascript, ReactJS
Office	L ^A T _E X, Microsoft Office, GIMP, Inkscape
Modelling & Simulation	MATLAB Simulink, OPAL-RT eFPGAsim, RT-XSG, RT-LAB, RTDS RSCAD, DPsim

Languages

German	Native
English	Fluent
Beginner	French

Interests

- Contributing to open-source software projects
- Sports: Running, Swimming, Cycling
- Hiking & Traveling: Scandinavia, Iceland, Greenland
- Tinkering / hacking with electronics & embedded device, home-automation
- Blogging: <https://www.noteblok.net>
- Build community-run ICT network infrastructure: Freifunk & dn42

Memberships

- IEEE Student Member
- Chaos Computer Club e.V.
- ROCK YOUR LIFE! Aachen e.V.
- Freifunk Rheinland e.V.

Publications & Contributions

For a full overview of personal and academic projects, take a look at my blog: www.noteblok.net.

Master thesis

Title *Development of a modular and fully-digital PCIe-based interface to Real-Time Digital Simulator*

Supervisor Marija Stevic

Examiner Prof. Antonello Monti

Grade 1.0

Bachelor thesis

Title *A generic memory management with paging for a minimalistic operating system*

Supervisor Dr. rer. nat. Stefan Lankes

Examiner Prof. Rudolf Mathar

Grade 1.0

Scientific articles & papers

- [1] A. Estebarsari, S. Vogel, R. Melloni, M. Stevic, E. Bompard, and A. Monti, "Frequency Control of Low Inertia Power Grids with Fuel Cell Systems in Distribution Networks," *IEEE Access*, pp. 1–1, 2022, Conference Name: IEEE Access, ISSN: 2169-3536. DOI: 10.1109/ACCESS.2022.3187099.
- [2] M. H. Syed, E. Guillo-Sansano, Y. Wang, *et al.*, "Real-Time Coupling of Geographically Distributed Research Infrastructures: Taxonomy, Overview and Real-World Smart Grid Applications," *IEEE Transactions on Smart Grid*, pp. 1–1, 2020, Conference Name: IEEE Transactions on Smart Grid, ISSN: 1949-3061. DOI: 10.1109/TSG.2020.3033070.
- [3] S. Vogel, H. T. Nguyen, M. Stevic, *et al.*, "Distributed Power Hardware-in-the-Loop Testing Using a Grid-Forming Converter as Power Interface," *en, Energies*, vol. 13, no. 15, p. 3770, Jan. 2020, tex.ids: vogelDistributedPowerHardwareintheLoop2020 number: 15 publisher: Multidisciplinary Digital Publishing Institute. DOI: 10.3390/en13153770. [Online]. Available: <https://www.mdpi.com/1996-1073/13/15/3770> (visited on 11/26/2020).
- [4] M. Mirz, S. Vogel, G. Reinke, and A. Monti, "DPsim—A dynamic phasor real-time simulator for power systems," *en, SoftwareX*, vol. 10, p. 100253, Jul. 2019, tex.ids: mirzDPsimDynamicPhasor2019, ISSN: 2352-7110. DOI: 10.1016/j.softx.2019.100253. [Online]. Available: <http://www.sciencedirect.com/science/article/pii/S2352711018302760> (visited on 11/26/2020).
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tionInterface2019 ISSN: 2577-1647, vol. 1, Oct. 2019, pp. 6655–6662. DOI: 10.1109/IECON.2019.8926918.

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- [9] A. Monti, M. Stevic, S. Vogel, *et al.*, “A Global Real-Time Superlab: Enabling High Penetration of Power Electronics in the Electric Grid,” *IEEE Power Electronics Magazine*, vol. 5, no. 3, pp. 35–44, Sep. 2018, tex.ids: montiGlobalRealTimeSuperlab2018, montiGlobalRealTimeSuperlab2018a conferenceName: IEEE Power Electronics Magazine, ISSN: 2329-9215. DOI: 10.1109/MPEL.2018.2850698.
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